1 ABOUT SNDS100 BOARD

SYSTEM OVERVIEW

SNDS100(Samsung NetARM Development System for KS32C50100/KS32C5000(A) is a platform that is suitable for code development of SAMSUNG's KS32C50100 16/32-bit RISC microcontroller(NetARM-II) for Ethernet-based system. Also it supports a development of KS32C5000(A)(NetARM-I) in a similar way as SNDS do.

KS32C50100/KS32C5000(A) consists of 16-/32-bit RISC(ARM7TDMI) CPU core, 8-Kbyte unified cache/SRAM, I2C-bus controller, Ethernet controller with 2-channel buffered DMA, 2 HDLC with 4-channel buffered DMA, 2-channel GDMA, 2 UARTs, two 32-bit timers, 18 programmable I/O ports, interrupt controller, and a system manager. it also supports JTAG boundary scan for the application system testing.

SNDS100 consists of KS32C50100/KS32C5000(A) , boot EEPROM(Flash ROM), DRAM module, SDRAM, serial ports for console, two serial communication ports, ethernet interface, configuration switches, and status LEDs/LCD. The Ethernet interface has a complete IEEE802.3 physical layer interface with ethernet hub/router side RJ45 connector configuration.

SNDS100 BOARD OVERVIEW

The SNDS100 shows the basic system-based hardware design which uses the KS32C50100/KS32C5000(A) . It can evaluate the basic operations of the KS32C50100/KS32C5000(A) and develop codes for it as well.

When the KS32C50100/KS32C5000(A) is contained in the SNDS100 , you can use an in-circuit emulator(ICE).

This allows you to test and debug a system design at the processor level. In addition, the KS32C50100/ KS32C5000(A) with embeddedICETM capability can be debugged directly using the EmbeddedICE Interface.

The SNDS100 function blocks are shown in Figure 1-1.

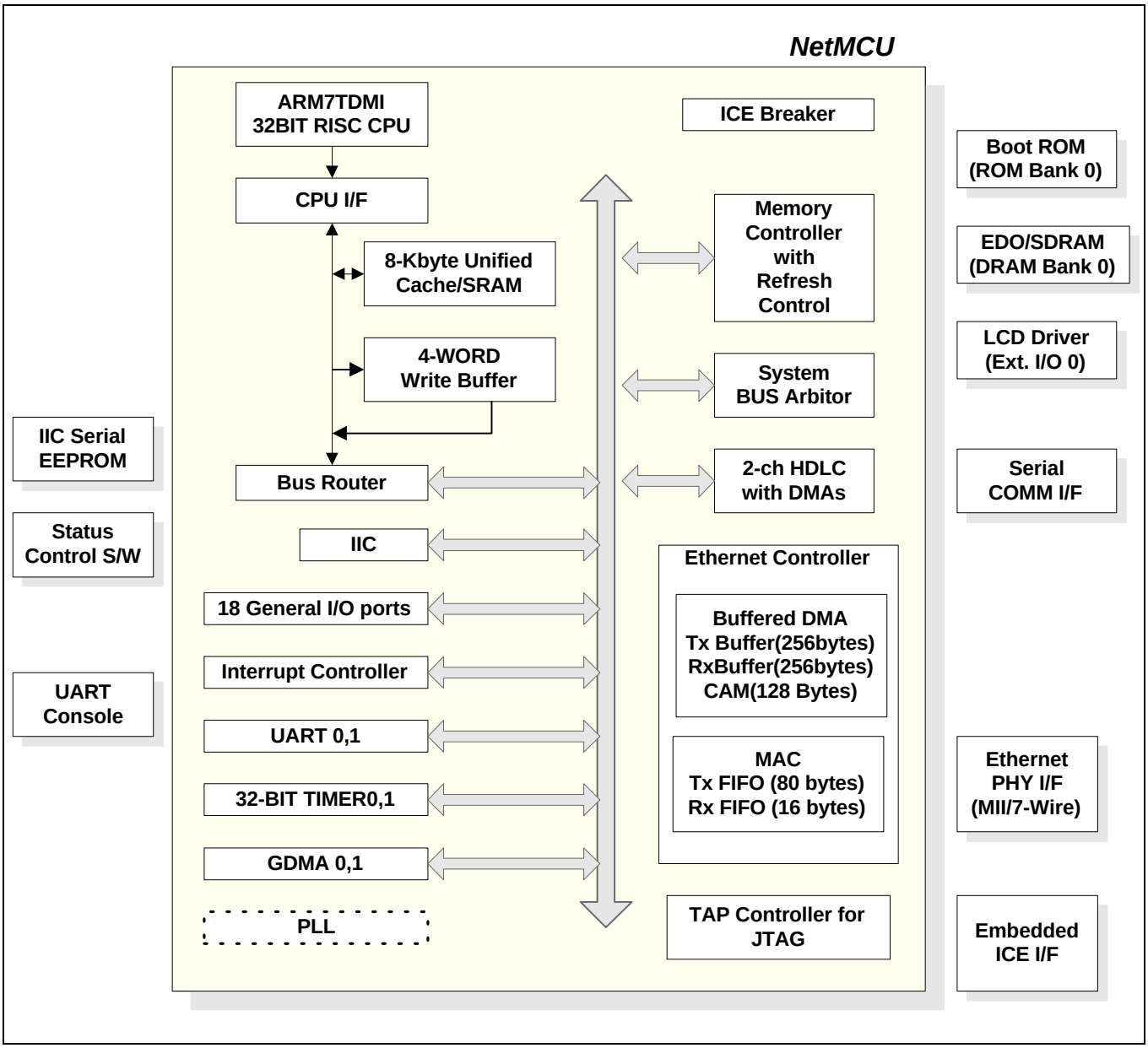


Figure 1-1. SNDS100 Block Diagram

FEATURES

— KS32C50100/KS32C5000(A) : 16/32-bit RISC microcontroller
— Boot ROM : 512K bit, 1M bit, 4M bit, support byte, half-word, word size boot ROM
— DRAM : 72-pin SIMM module with two banks and EDO DRAM support
— SDRAM : Two 4Mx16 with 2banks SDRAM support
— External I/O : status LCD driver
— General I/O : control switches and status display LED
— Two serial ports, one for console
— I2C-bus EEPROM
— Two-channel serial communication interface
— 10/100Mbps Ethernet interface
— EmbeddedICE™ Interface

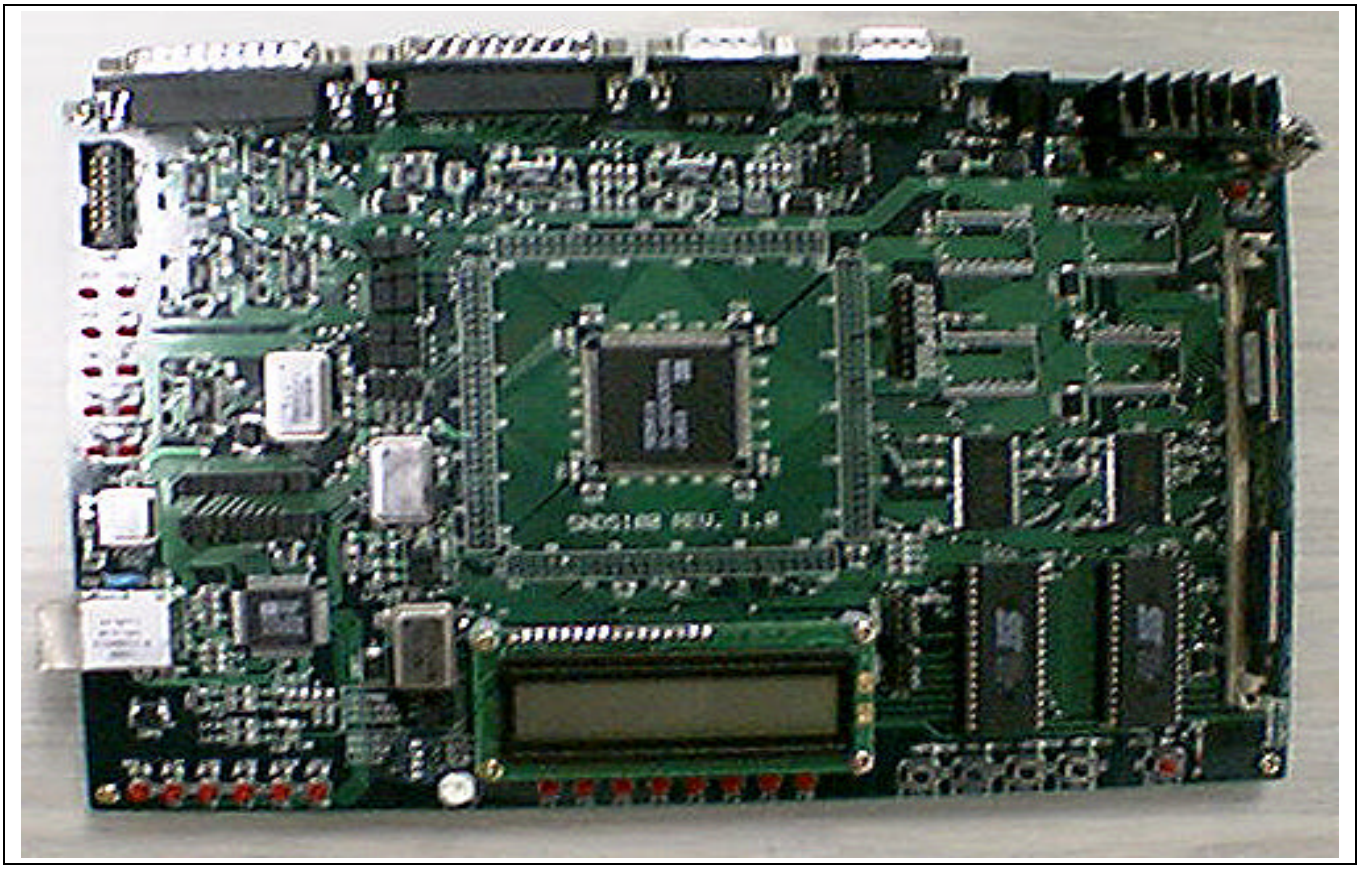


Figure 1-2. SNDS100 Rev1.0 Evaluation Board

CIRCUIT DESCRIPTION

SNDS100 board consists of logic components, several control/status display block, and a debug interface block. SNDS100 board's detailed block diagram, and its components are shown in figure 1-4. SNDS100 board schematics are inserted at the end of this section.

POWER SUPPLY

SNDS100 is designed to operate at 3.3V and 5V. Power to the SNDS100 is supplied through a DC jack power adapter which supports the voltage between 6V and 9V and drives the current at least 850 mA .

SNDS100 board has distributed power plane, with power going separately to the MCU and the main power plane. In case of KS32C5000(A), main power and MCU power has 5V level. But with KS32C50100,MCU power has 3.3V. For this reason, power jumpers J5,J6,J7 and J8 are inserted (see Figure 1-3) .

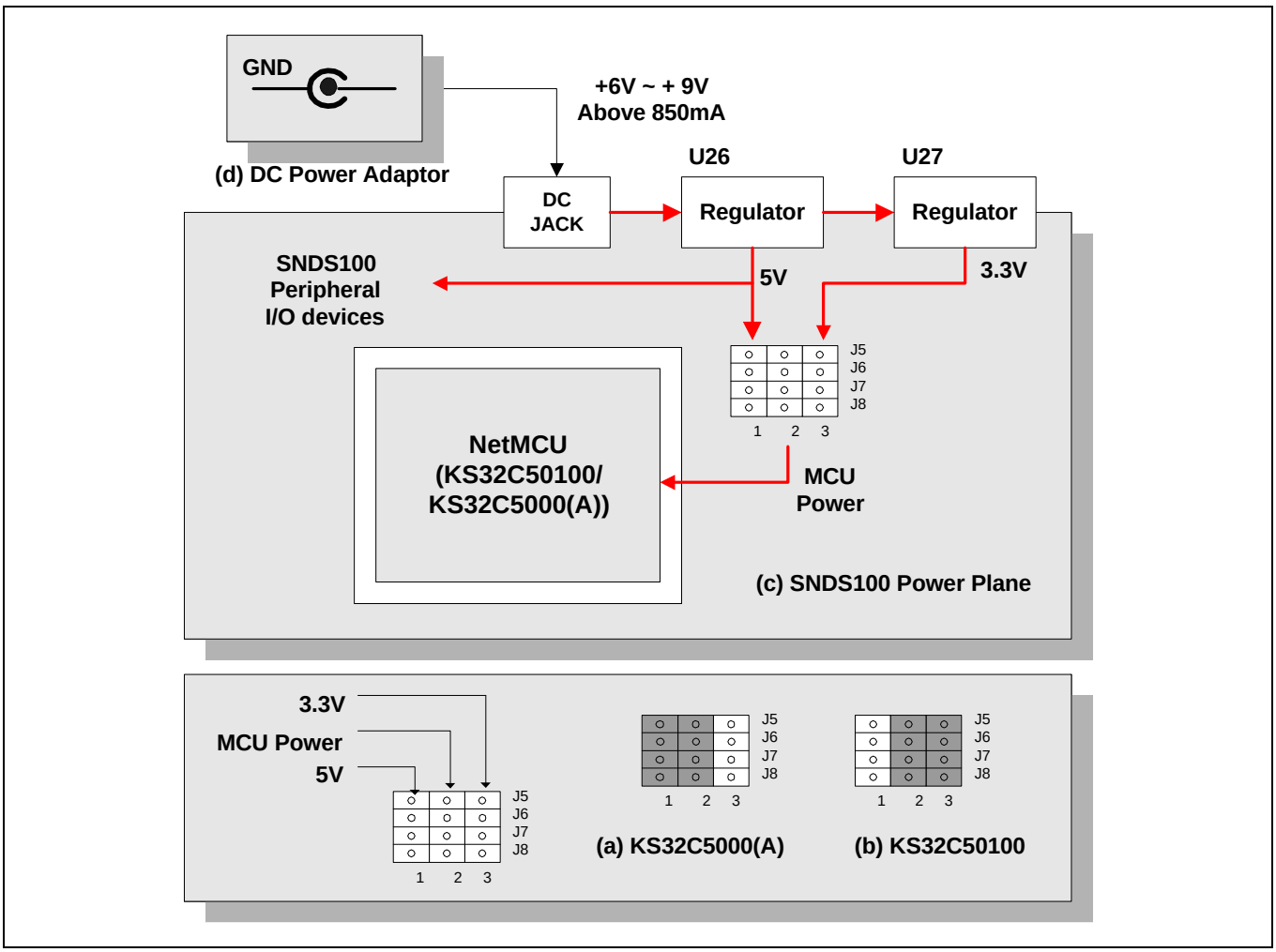


Figure 1-3. SNDS100 Power Plane

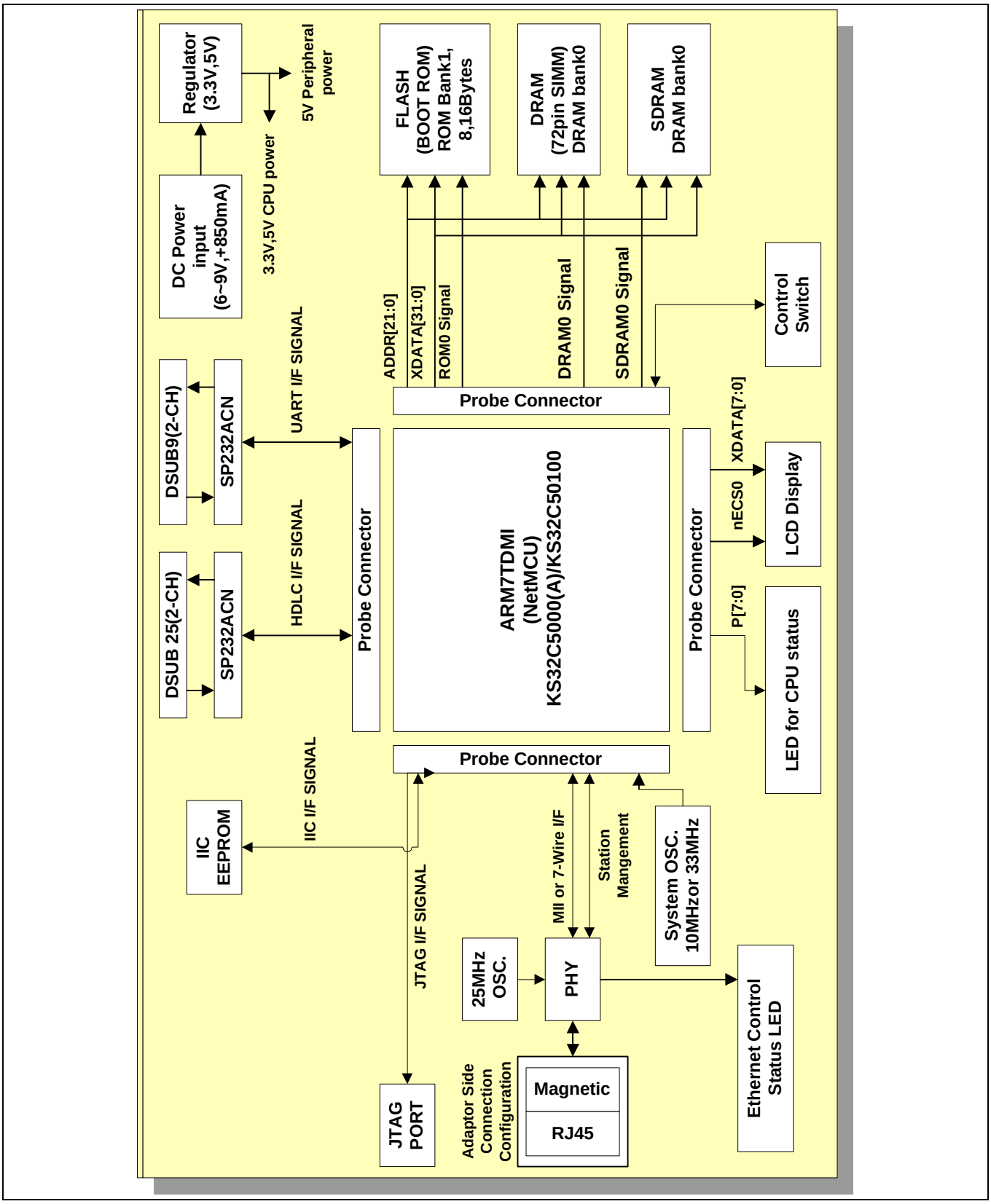


Figure 1-4. Detailed SNDS100 Board Diagram

CLOCK SOURCE AND DISTRIBUTION

The Following clock sources are supported at SNDS100 target board.

System Clock (MCLK)

In case of that the attached device on SNDS100 is KS32C5000(A), then you can use 33MHz oscillator for system clock source. If KS32C50100 device is attached on it, then you can directly assign the 50MHz oscillator to the MCLK input pin or 10MHz with PLL enabled. (See, Figure 1-5)

System Clock Out (MCLKO)

MCLKO is the same signal as internal system clock(MCLK) of KS32C50100/5000(A). This clock can be monitored at MCLKO pin as to assign high to CLKOEN(MCKO clock output enable/disable input) pin . If you want to use SDRAM with KS32C50100, MCLKO should be used. (See, Figure 1-5)

Table 1-1. System clock configurations

DEVICE	JUMPER	1-2(HIGH)	2-3(LOW)	NOTE
KS32C50100/ KS32C5000(A)	TMOD(J2)	(Don' t use)	Normal	Should be set to LOW for normal operation.
KS32C5000(A)	CLKSEL(J3)	MCLK/2	MCLK	SYSTEM Clock(MCLK) select input pin.
KS32C50100		MCLK	PLL output	MCLK input frequency can be controlled by this pin.
KS32C50100/ KS32C5000(A)	CLKOEN(J4)	MCLKO enabled	MCLKO disabled	MCLKO have to be enabled to use SDRAM(only for KS32C50100)

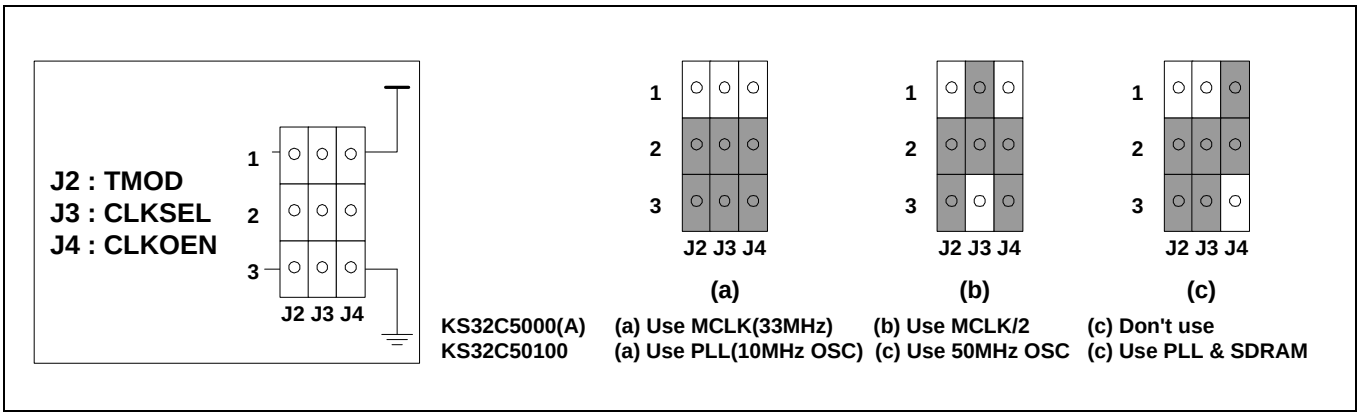


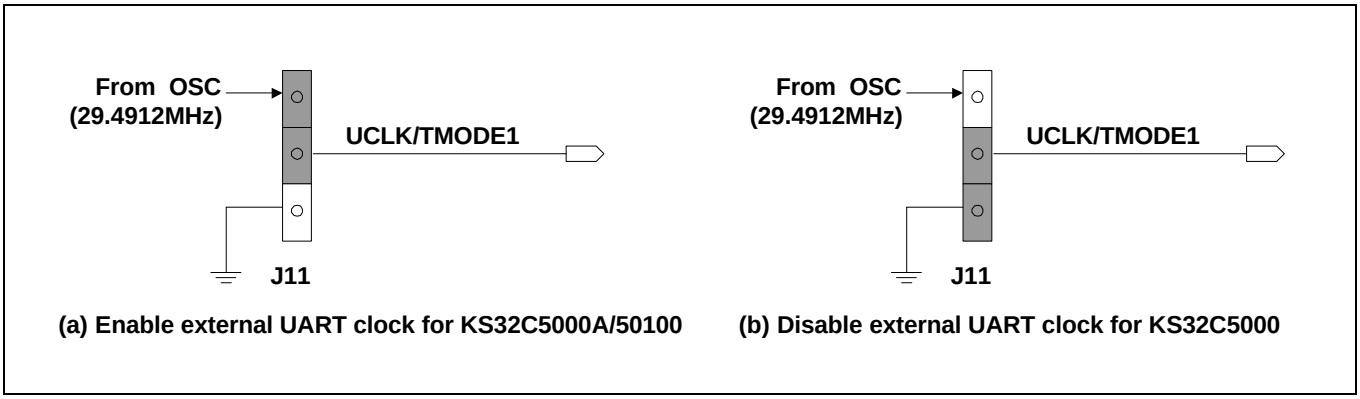
Figure 1-5. The Examples of System Clock(MCLK) Configurations

Ethernet Control Clock

25MHz crystal oscillator have to be used for 100/10Mbps Ethernet PHY control clock.

External UART Clock

KS32C50100/5000A support the External UART Clock input pin (UCLK[64]). If you using KS32C5000 with SNDS100, This UCLK input pin have to be assigned to LOW. Because it is used as the test mode selection pin(TMOD1) for KS32C5000. (see Figure 1-6).



(a) Enable external UART clock for KS32C5000A/50100 **(b) Disable external UART clock for KS32C5000**

Figure 1-6. External UART Clock Configurations

RESET LOGIC

The nRESET(System Reset Signal) must be held to low level at least 540 master clock cycles to reset a KS32C50100/5000(A). nRESET and nTRST(JTAG Reset signal) is logic anded. But, if you want to use circuit emulator(ex, Embedded ICE) for dubug without BOOT ROM, you should have the nTRST is floated. If not, whenever the ADW(ARM Debug Window) were invoked SW interrupt will be occurred.

Therefore, the current SNDS100 Rev.1.0 schematic for reset logic have to be updated. It is referred to “Section 4. JTAG for Embedded ICE Interface” .

SNDS100 SYSTEM CONFIGURATIONS

SNDS100 board provides Big-/Little- endian mode with KS32C50100/5000A and supports Byte/Halfword/Word access the data bus.

Are you using KS32C5000(A) on SNDS100 board?. Then you have to pull-out the all jumper from J9. Because of these pins are CPU monitoring pins(CPUMP[2:0]) of KS32C5000(A). But, in case of KS32C50100, these pin functions are changed to the filter input and analog power for the internal PLL circuit. See the schematic file which is at the end of this section.

Flash Boot ROM

DIP type ROM sockets(U17, U18) are on SNDS100 for to support the byte(8 bits) or halfword(16 bits) BOOT ROM even though the data bus for ROM Bank0 can be configured by B0SIZE[1:0] pins up to 32bit.

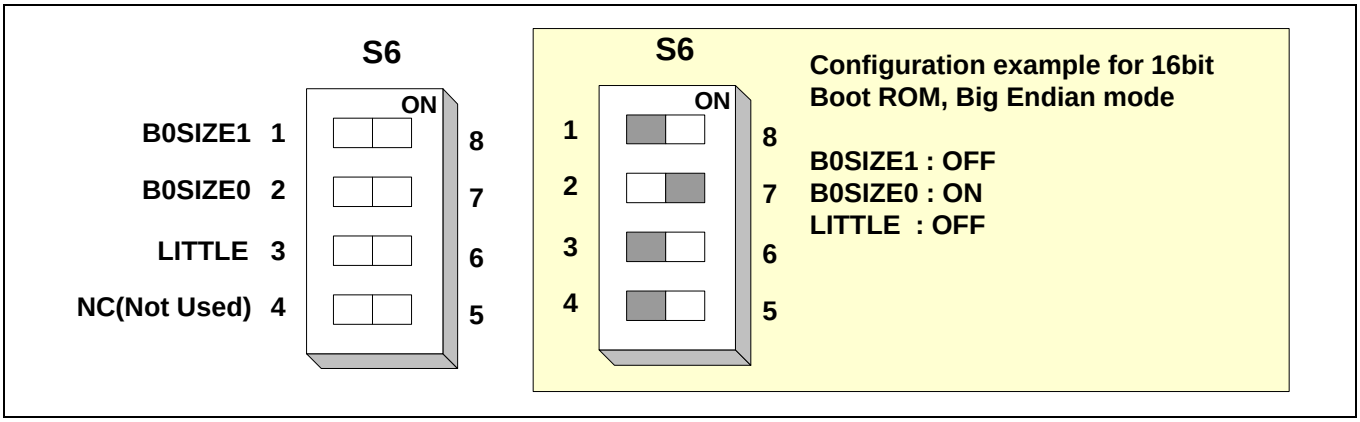


Figure 1-7. SNDS100 Board Configurations

Table 1-2. ROM Bank0 Data Bus Width

PIN FUNCTIONS	S6: B0SIZE[1:0]	PIN VALUE	DESCRIPTIONS
ROM Bank0 Data Bus Width configuration	ON, ON	"00"	Reserved
	ON,OFF	"01"	Byte (8 bits)
	OFF,ON	"10"	Half-word (16 bits)
	OFF,OFF	"11"	Word (32 bits)

Table 1-3. Endian Mode Configuration

PIN FUNCTIONS	S6: LITTLE	PIN VALUE	DESCRIPTIONS
Endian Mode Selection	ON	"1"	Little endian mode (KS32C50100/KS32C5000A)
	OFF	"0"	Big endian mode. KS32C5000 is fixed to this mode.

DRAM/SDRAM Configurations

SNDS100 has the 72-pin SIMM module on the board for one bank DRAM. KS32C50100 can support Synchronous DRAM(SDRAM). In this case, SDRAM or DRAM memory can be selected alternatively using by SYSCFG register. KS32C5000(A) did not support SDRAM type. Using these device with SNDS100, JP2 have to be set to select DRAM.

Bank select jumper for DRAM/SDRAM, JP2/JP1 on SNDS100 are provided just only for the purpose of each bank test. So, you want to use SDRAM, you have to enable a SDRAM bank and remove same DRAM bank' s jumper.

BOOT ROM code find out the type of memory which is installed on SNDS100 , and then initialize the memory banks, base/end pointer and the timing of CAS/RAS after the system power on reset or the reset key pressed and released. If DRAM banks are found, each bank can be configured as an EDO DRAM mode using the system management block DRAM bank control register.

ROM and External I/O Bank Chip Select Jumpers(J8)

SNDS100 also provides ROM and External I/O bank selection jumper for the purpose of each bank test using by SRAM(U20, U21, U19, U22).

— RS1 ~ R25 : ROM/SRAM/FLASH bank selection jumpers.

— ES0 ~ ES3 : External I/O bank selection jumpers.

These bank selection jumper(J8) have to be enabled only one bank, if you want to use it.

STATUS LCD DRIVER

SNDS100 provide LCD display to indicate SNDS100 status. External I/O bank 0 is used to control the LCD driver. The LCD Driver interface connector pin numbers are described in Table 1-4.

Table 1-4. LCD Driver Interface

Pin No.	Descriptions
1	GND
2	VCC
3	Resolution control
4	A[1]
5	A[0]
6	Chip select
[14:7]	DATA[7:0]

GENERAL I/O PORTS

KS32C50100/KS32C5000(A) 's general I/O ports are used for SNDS100 key interrupt input and LED status display. The function of control switch and the status of LED can be defined by user software.

Table 1-5. General I/O Configurations on SNDS100

General I/O port number	I/O type	Descriptions
P[7:0]	Output	LED display
P[11:8]	Input	Key input pad (External interrupt input pins).
P[17:16]	Output	HDLC Data Set Ready Signal output(nDSRB/nDSRA).

ETHERNET INTERFACE

KS32C50100/KS32C5000(A) has one 10-/100-Mbps Ethernet controller. SNDS100 supports 10-/100-Mbps Ethernet interface, A PHY chip set used in SNDS100 is able to operate 10-/100-M bps using auto-negotiation and communicate with KS32C50100/KS32C5000(A) using an MII interface.

SNDS100 Ethernet connector(RJ45) has Ethernet adapter side pin configuration which supports communication between the SNDS100 and the host PC's NIC. You can connect SNDS100 to hub or router direct without twisting cable. Both receive and transmit domains must be connected to the digital domain through a ferrite bead or inductor. The value of the inductor is from 0.1uH to 1uH.

Jumpers(J3-1,J3-2) are located between the MII interface of NetMCU MAC and PHY for another PHY chip. User who would like to use any other vendor' s PHY chip can use this jumpers as interface a daughter board. These jumpers should be always enabled for MAC evaluation.

The PCB power plane and RJ45 connector(J1) configurations are shown in Figure 1-8.

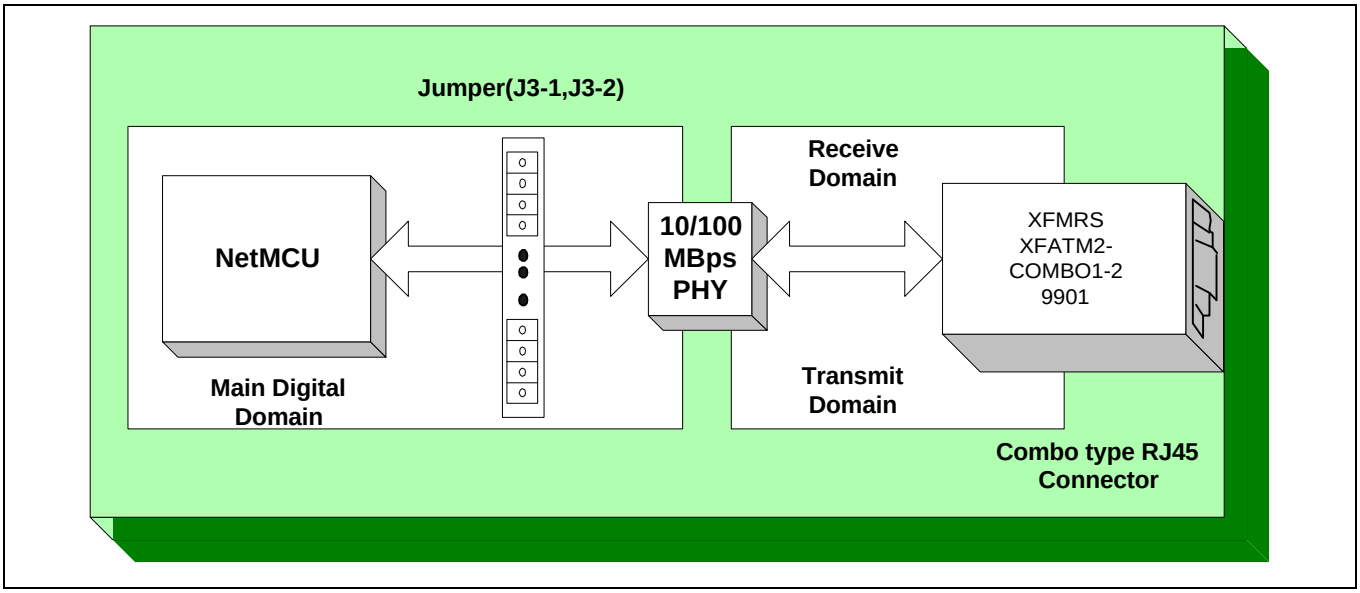


Figure 1-8. Ethernet I/F PCB Power Plane on SNDS100

Table 1-6. RJ45 Pin Configurations for Adapter side

Pin Number	Descriptions	Pin Number	Descriptions
1	CMT	5	NC
2	CT_T	6	CT_R
3	TX+	7	RX+
4	TX-	8	RX-

Ethernet Status LED

— LED location : D1, D2, D3, D4, D5

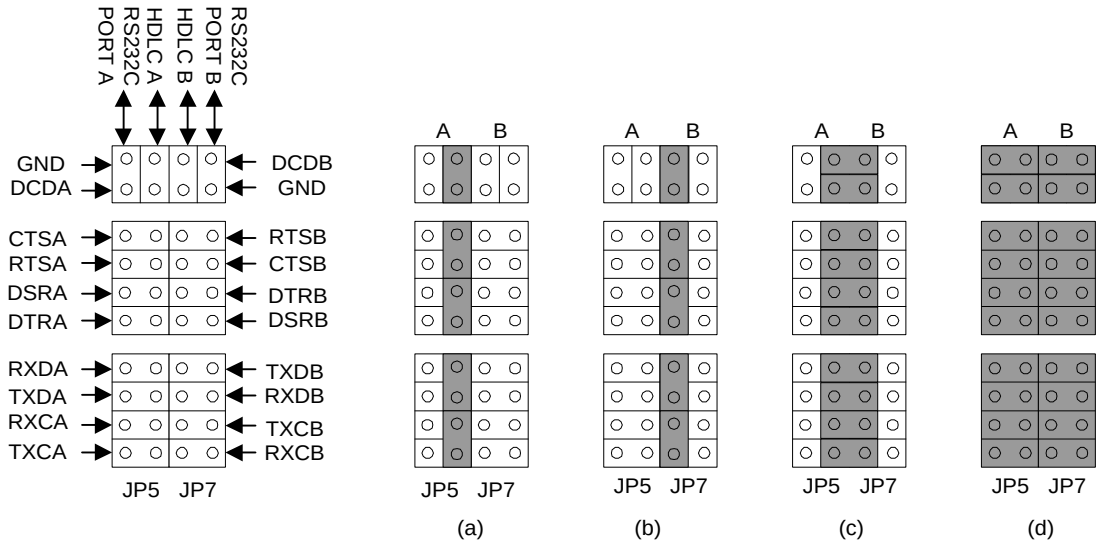
— Indicate the line status, operation mode and Speed.

Table 1-7. Ethernet Status LED.

LED	FUNCTIONS	DESCRIPTIONS
D1	ACTIVITY	Line Status LED. Indicate Full-Duplex operation.
D2	RX	Receive data LED.
D3	TX	Transmit data LED.
D4	LI	Link integrity LED.
D5	COL	Collision detected.
	SPEED	Activity LED. Indicate 100Mbps operation.

HDLC TEST CIRCUIT CONFIGURATIONS

SNDS100 board provides HDLC external loop back test jumper(JP5,JP6,JP7). Configuring the jumper set, you can test the external loop back between the HDLC channel. Also you can select the HDLC Oscillator for external HDLC clock input using by JP6.



(a) HDLC-A channel external loop back test (From channel A to A)
(b) HDLC-B channel external loop back test (From channel B to B)
(c) HDLC channel A to B external loop back test (From channel A to B or B to A)
(d) HDLC channel A to B external test (Interface with V.24/RS232)

Figure 1-9. HDLC Jumper Setting for External Loop Back Test

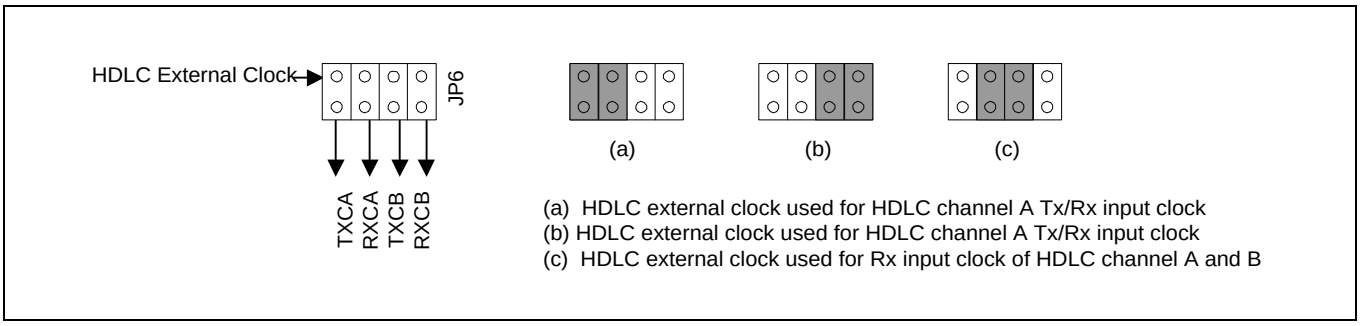


Figure 1-10. HDLC Tx/Rx Clock Input Configurations

Serial (HDLC, UART) & JTAG Interface

SNDS100 board supports the two 9DIP SUB serial connector for two channel UART(P2A SIO-0, P2B SIO-1). If you want to get the connector pin configurations, please refer to "Section 2".

NetMCU device have the two-channel HDLC(High Level Data Link Controllers) for serial communication. The SNDS100 provides serial communication port(HDLC-A P1A, HDLC-B P1B) with V.24/RS-232 interface.

SNDS100 support JTAG port. It can be used as Circuit emulator(ex, Embedded ICE) interface for boundary scan test and debugging channel for application. For the details, See the "Section 4. System design".

SNDS100 REV. 1.0. BOARD SCHEMATICS

1. MAIN.SCH : SNDS100 TOP SCHEMATIC
2. MCU.SCH : NetMCU(KS32C50100/5000(A)) device interface
3. SYSTEM.SCH : REV. 1.0
4. SYSTEM.SCH : REV. 1.1
5. DRAM.SCH : DRAM/SDRAM SCHEMATICS
6. ETHERNET.SCH
7. EXTERNAL.SCH
8. HDLC.SCH : REV. 1.0
9. HDLC.SCH : REV. 1.1
10. ROM.SCH
11. SRAM.SCH
12. UART.SCH : REV. 1.0
13. UART.SCH : REV. 1.1
14. Bill Of Materials

BILL OF MATERIALS OF SNDS100 REV1.0

SNDS100(Samsung NetMCU Development System) Revised: Saturday, January 16, 1999
MAIN.SCH Revision: 1.0

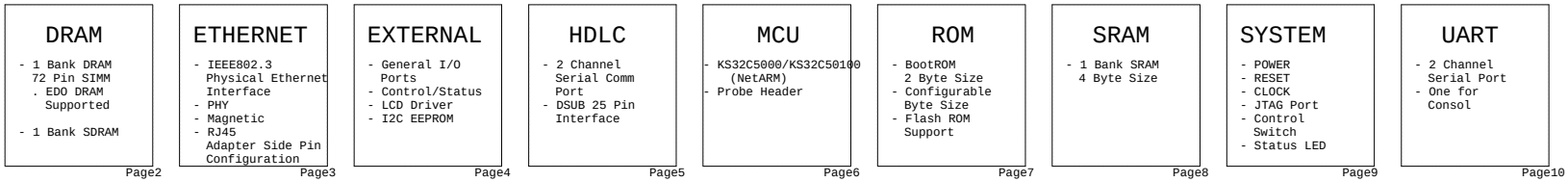
KIMS TECHNOLOGY CO.
#H-305 Konggu sangga ilbeongi
#636-62, Kuro-Dong, Kuro-Gu
Seoul, Korea 152-050
E-mail: kimstek@unitel.co.kr

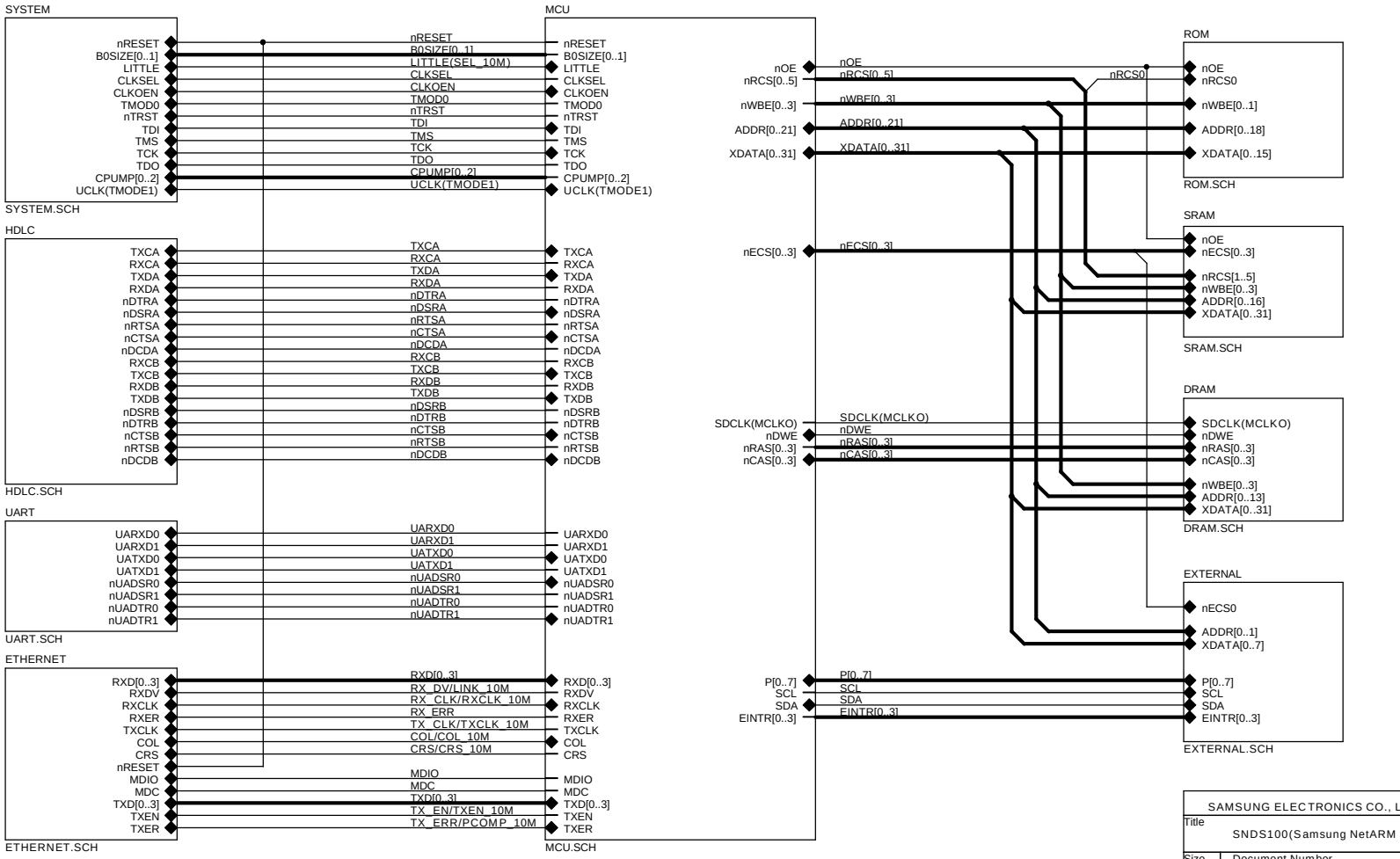
Bill Of Materials March 5,1999 12:22:22 Page1

Item	Quantity	Reference	Part
1	98	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C25, C26, C27, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C94, C98, C99, C100, C101, C102, C103, C104, C109, C110, C111, C112, C113, C114	0.1uF
2	1	C22	0.001uF/2KV
3	5	C23, C24, C28, C91, C120	10uF
4	1	C90	10uF/16V
5	1	C92	0.1uF
6	1	C93	820pF
7	1	C95	100uF/6.3V
8	1	C96	100uF/16V
9	1	C97	100uF/10V
10	8	C105, C106, C107, C108, C115, C116, C117, C118	330pF
11	25	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D26, D27	LED
12	1	D24	1N4148
13	1	D25	1N4004
14	3	JP1, JP2, JP6	HEADER 4x2
15	2	JP5, JP7	HEADER 10x2
16	1	JP8	HEADER 9x2
17	1	JP9	HEADER 3x2
18	1	JP10	HEADER 7x2
19	1	J1	XFATM2-COMBO-4
20	8	J2, J3, J4, J5, J6, J7, J8, J11	CON3

Item	Quantity	Reference	Part
21	2	J9, J12	CON1
22	1	J10	DC_JACK
23	4	J2-1, J2-2, J2-3, J2-4	HEADER 26x2
24	2	J3-1, J3-2	HEADER 11x2
25	9	L1, L2, L3, L4, L5, L6, L7, L9, L11	F.B
26	2	P1A, P1B	CONNECTOR DB25
27	1	P2	CONNECTOR DB9x2
28	12	R1, R2, R3, R4, R5, R6, R21, R47, R49, R51, R57, R61	22
29	16	R7, R8, R9, R10, R11, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R58	680
30	2	R13, R14	49.9
31	1	R15	22K 1%
32	1	R17	100
33	2	R18, R59	1K
34	3	R19, R34, R35	2K
35	4	R20, R28, R52, R60	10K
36	8	R22, R23, R24, R25, R26, R27, R29, R30	330
37	9	R31, R32, R33, R36, R48, R50, R54, R55, R56	4.7K
38	1	R53	33
39	5	S1, S2, S3, S4, S5	SW PUSHBOTTON
40	1	S6	SW_DIP4
41	1	S7	SW ON/OFF
42	2	U1, U2	KM416S4020B
43	1	U3	DRAM_SIMM
44	1	U4	LEVELONE
45	1	U5	OSC(25MHz)
46	2	U6, U23	7414
47	1	U7	LCON14
48	1	U8	KS24C641
49	7	U9, U10, U11, U12, U13, U28, U29	MAX232
50	3	U14, U16, U25	OSC
51	1	U15	KS32C50100
52	2	U17, U18	29E010
53	4	U19, U20, U21, U22	KS681000C_55(SOP)
54	1	U24	7408
55	1	U26	78R05
56	1	U27	78R33

SNDS100 Board Ver1.0 (for NetARM : KS32C5000/KS32C50100)





SAMSUNG ELECTRONICS CO., LTD.		
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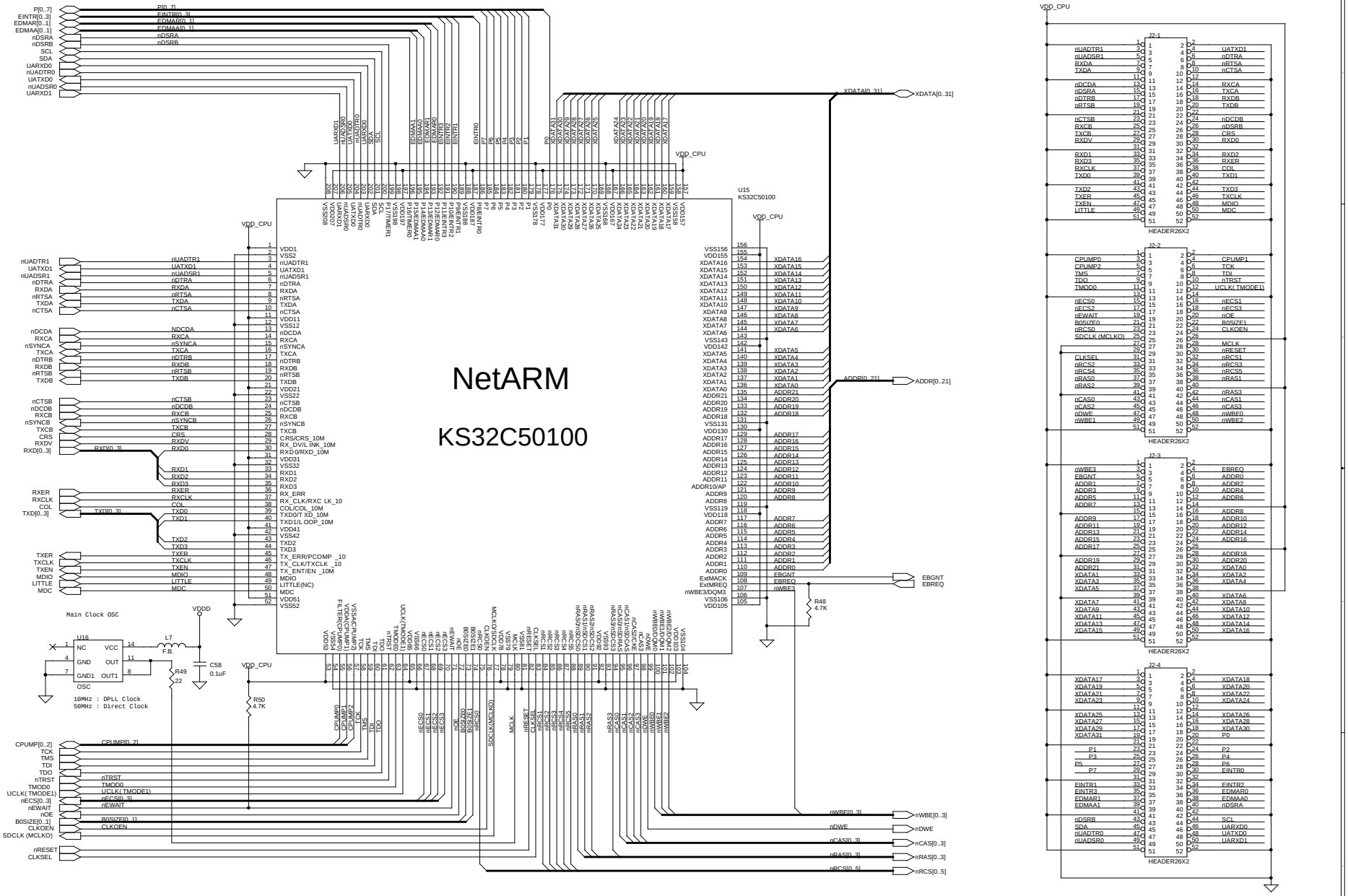
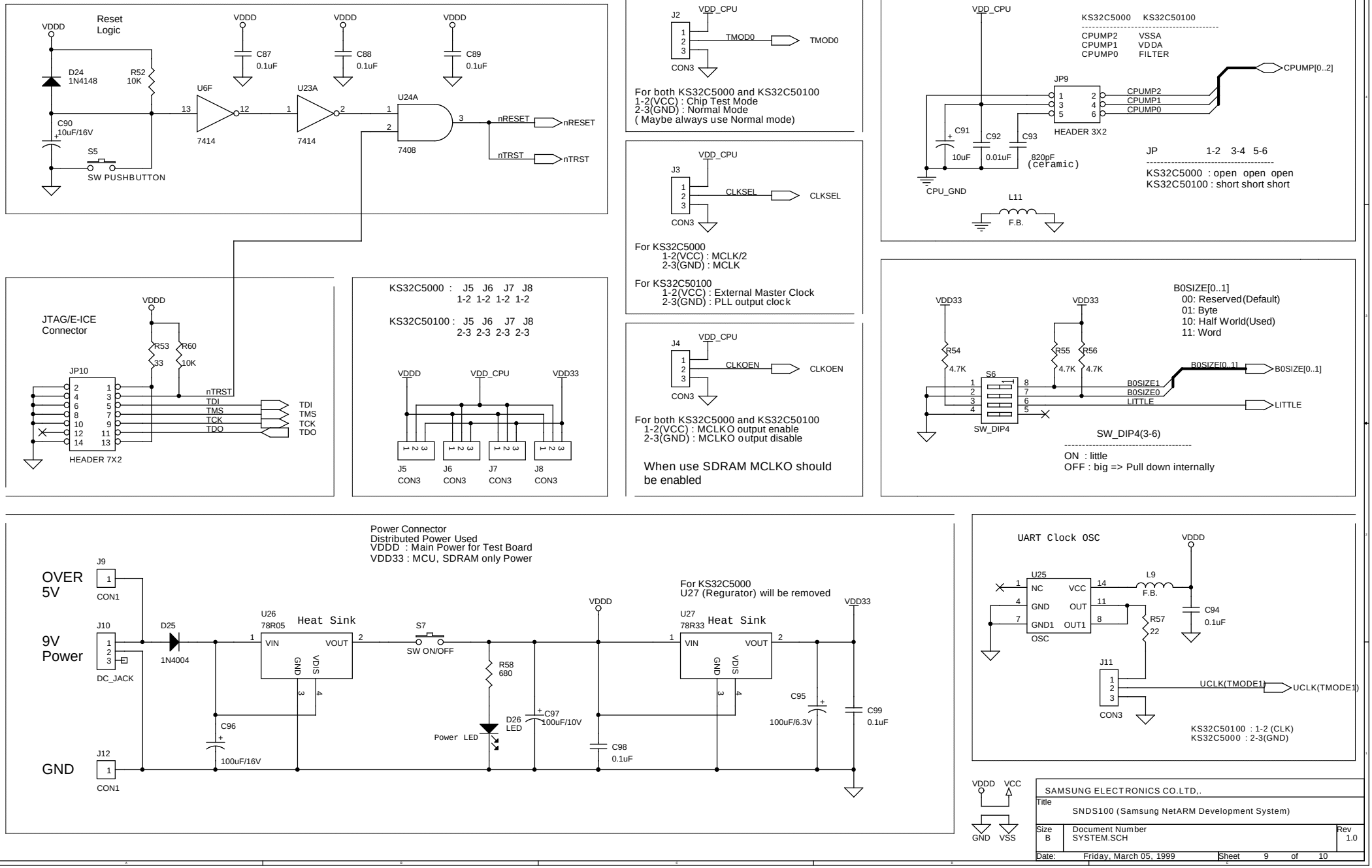
Size: B	Document Number: MAIN.SCH	Rev: 1.0
Date: Friday, March 05, 1999	Sheet 1 of 10	


NetARM
KS32C50100
U15
KS32C50100
Main Clock OSC
OSC
10MHz : DPLL Clock
50MHz : Direct Clock
HEADER26X2
SAMSUNG ELECTRO NICS CO.LTD.,
SNDS100 (Samsung NetA RM Development System)
MCU.SCH
Saturday, January 1 6, 1999


Reset Logic
VDDD
D24 1N4148
R52 10K
C90 10uF/16V
S5
SW PUSHBUTTON
C87 0.1uF
C88 0.1uF
C89 0.1uF
U6F
U23A
U24A
7414
7414
7408
nRESET
nTRST
JTAG/E-ICE Connector
JP10
R53 33
R60 10K
HEADER 7X2
TDI
TMS
TCK
TDO
KS32C5000 : J5 J6 J7 J8
1-2 1-2 1-2 1-2
KS32C50100 : J5 J6 J7 J8
2-3 2-3 2-3 2-3
VDD_CPU
VDD33
J5 J6 J7 J8
CON3
J2
TMOD0
For both KS32C5000 and KS32C50100
1-2(VCC) : Chip Test Mode
2-3(GND) : Normal Mode
(Maybe always use Normal mode)
J3
CLKSEL
For KS32C5000
1-2(VCC) : MCLK/2
2-3(GND) : MCLK
For KS32C50100
1-2(VCC) : External Master Clock
2-3(GND) : PLL output clock
J4
CLKOEN
For both KS32C5000 and KS32C50100
1-2(VCC) : MCLKO output enable
2-3(GND) : MCLKO output disable
When use SDRAM MCLKO should be enabled
KS32C5000 KS32C50100
CPUMP2 VSSA
CPUMP1 VDDA
CPUMP0 FILTER
JP9
HEADER 3X2
CPUMP[0..2]
C91 10uF
C92 0.01uF
C93 820pF (ceramic)
CPU_GND
L11
F.B.
JP 1-2 3-4 5-6
KS32C5000 : open open open
KS32C50100 : short short short
B0SIZE[0..1]
00: Reserved(Default)
01: Byte
10: Half World(Used)
11: Word
R54 4.7K
R55 4.7K
R56 4.7K
S6
SW_DIP4
B0SIZE1
B0SIZE0
LITTLE
SW_DIP4(3-6)
ON : little
OFF : big => Pull down internally
Power Connector
Distributed Power Used
VDDD : Main Power for Test Board
VDD33 : MCU, SDRAM only Power
OVER 5V
9V Power
GND
J9
J10
J12
CON1
DC_JACK
D25 1N4004
U26 78R05 Heat Sink
VIN
VOUT
GND
VDIS
S7 SW ON/OFF
R58 680
D26 LED
Power LED
C96 100uF/16V
C97 100uF/10V
C98 0.1uF
For KS32C5000
U27 (Regurator) will be removed
U27 78R33 Heat Sink
C95 100uF/6.3V
C99 0.1uF
UART Clock OSC
U25
NC
VCC
GND
OUT
GND1
OUT1
OSC
L9
F.B.
C94 0.1uF
R57 22
J11
UCLK(TMODE1)
KS32C50100 : 1-2 (CLK)
KS32C5000 : 2-3(GND)
VDDD VCC
GND VSS
SAMSUNG ELECTRONICS CO.LTD,.
Title
SNDS100 (Samsung NetARM Development System)
Size B
Document Number SYSTEM.SCH
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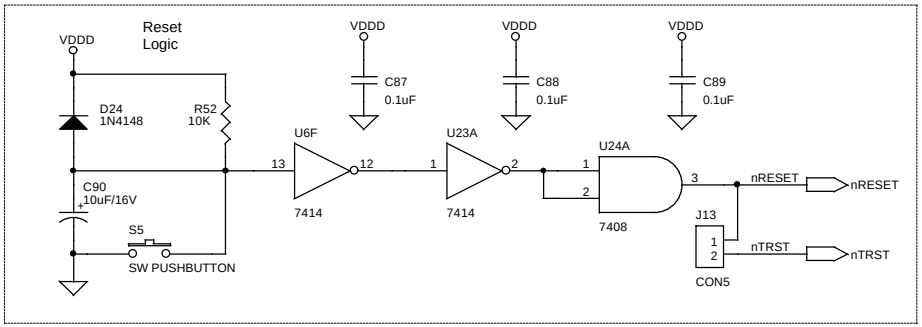
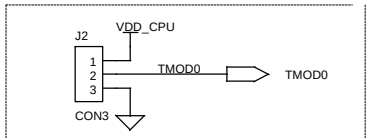
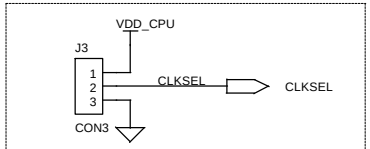


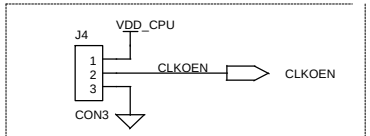


For both KS32C5000 and KS32C50100
1-2(VCC) : Chip Test Mode
2-3(GND) : Normal Mode
(Maybe always use Normal mode)



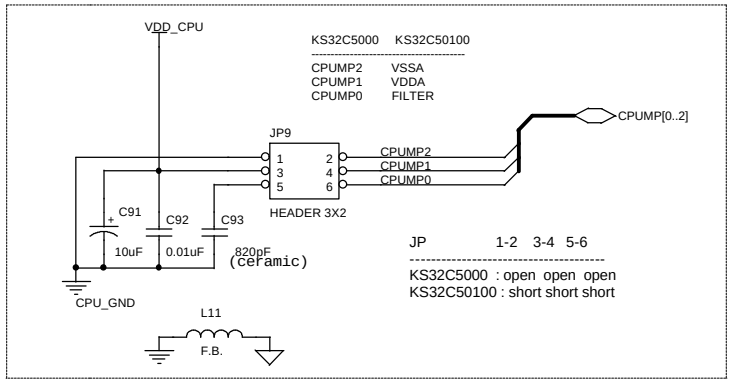
For KS32C5000
1-2(VCC) : MCLK/2
2-3(GND) : MCLK

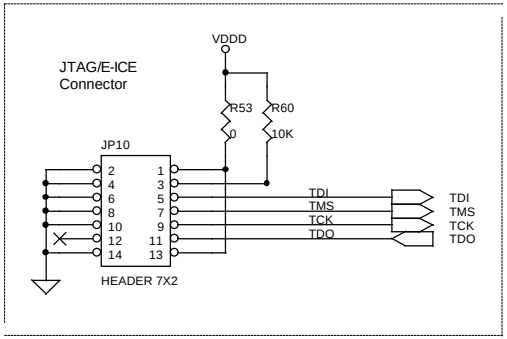
For KS32C50100
1-2(VCC) : External Master Clock
2-3(GND) : PLL output clock



For both KS32C5000 and KS32C50100
1-2(VCC) : MCLKO output enable
2-3(GND) : MCLKO output disable

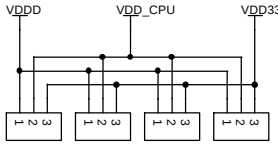
When use SDRAM MCLKO should be enabled

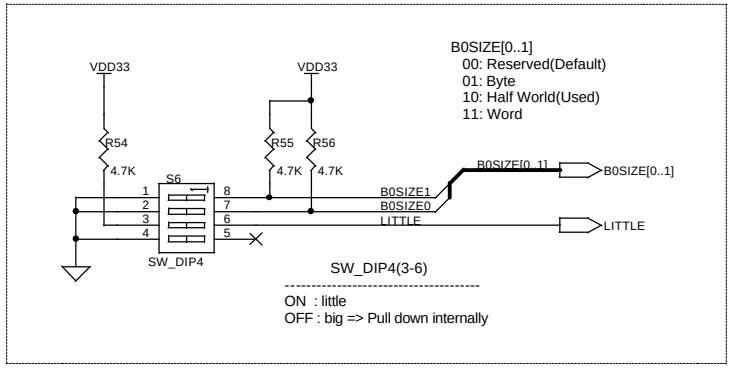




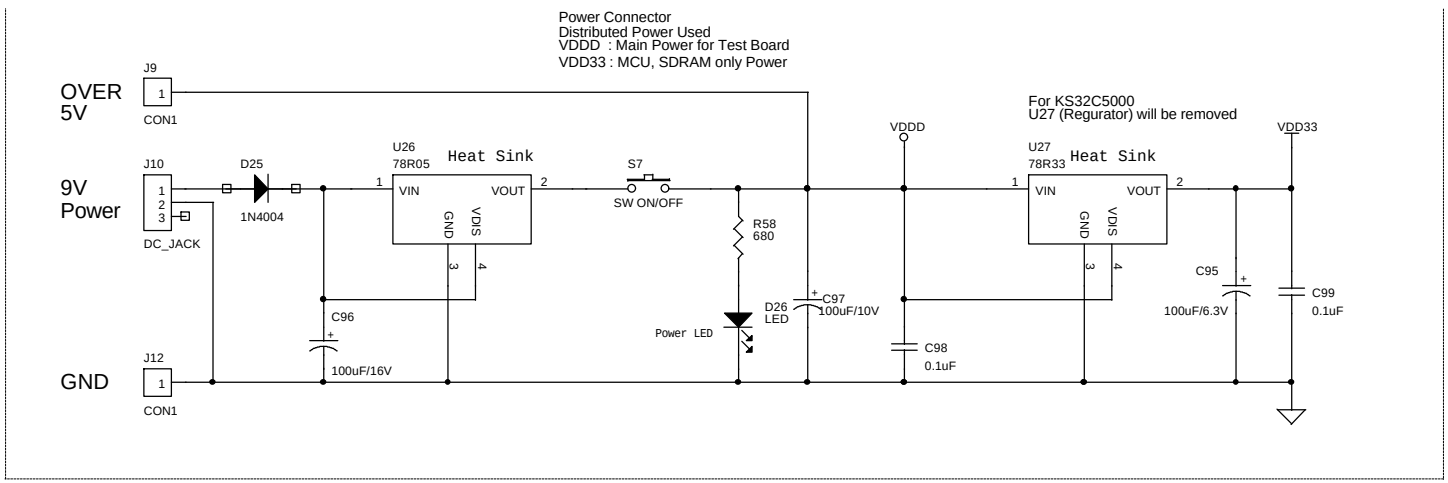
KS32C5000 : J5 J6 J7 J8
1-2 1-2 1-2 1-2

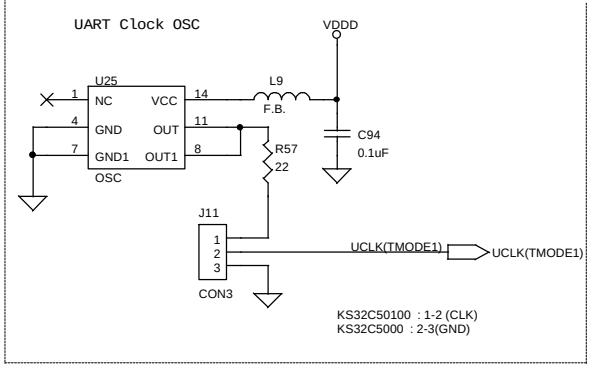
KS32C50100 : J5 J6 J7 J8
2-3 2-3 2-3 2-3





B0SIZE[0..1]
00: Reserved(Default)
01: Byte
10: Half World(Used)
11: Word





SAMSUNG ELECTRONICS CO.LTD,.		
Title: SNDS100 (Samsung NetARM Development System)		
Size: B	Document Number: SYSTEM.SCH	Rev: 1.1
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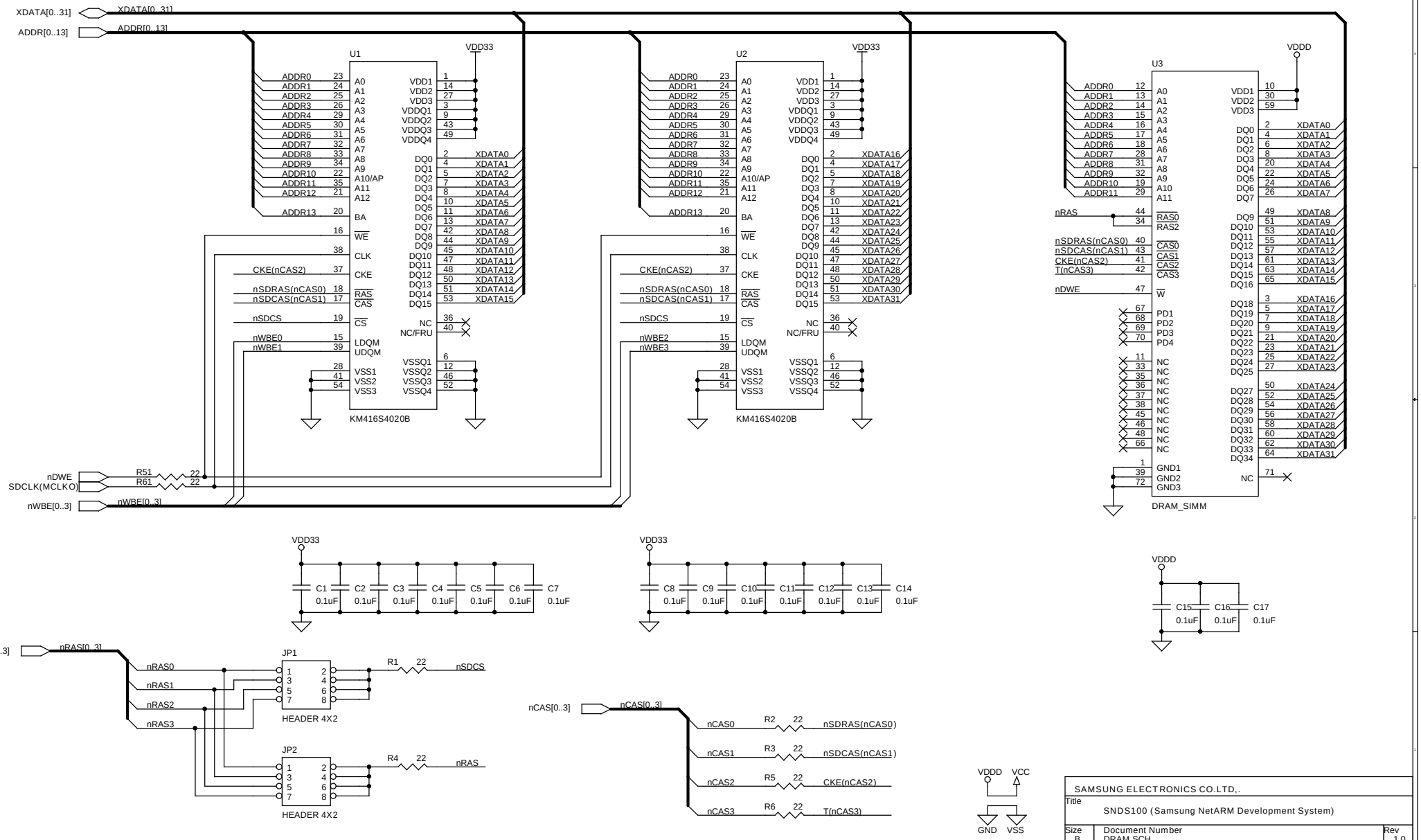
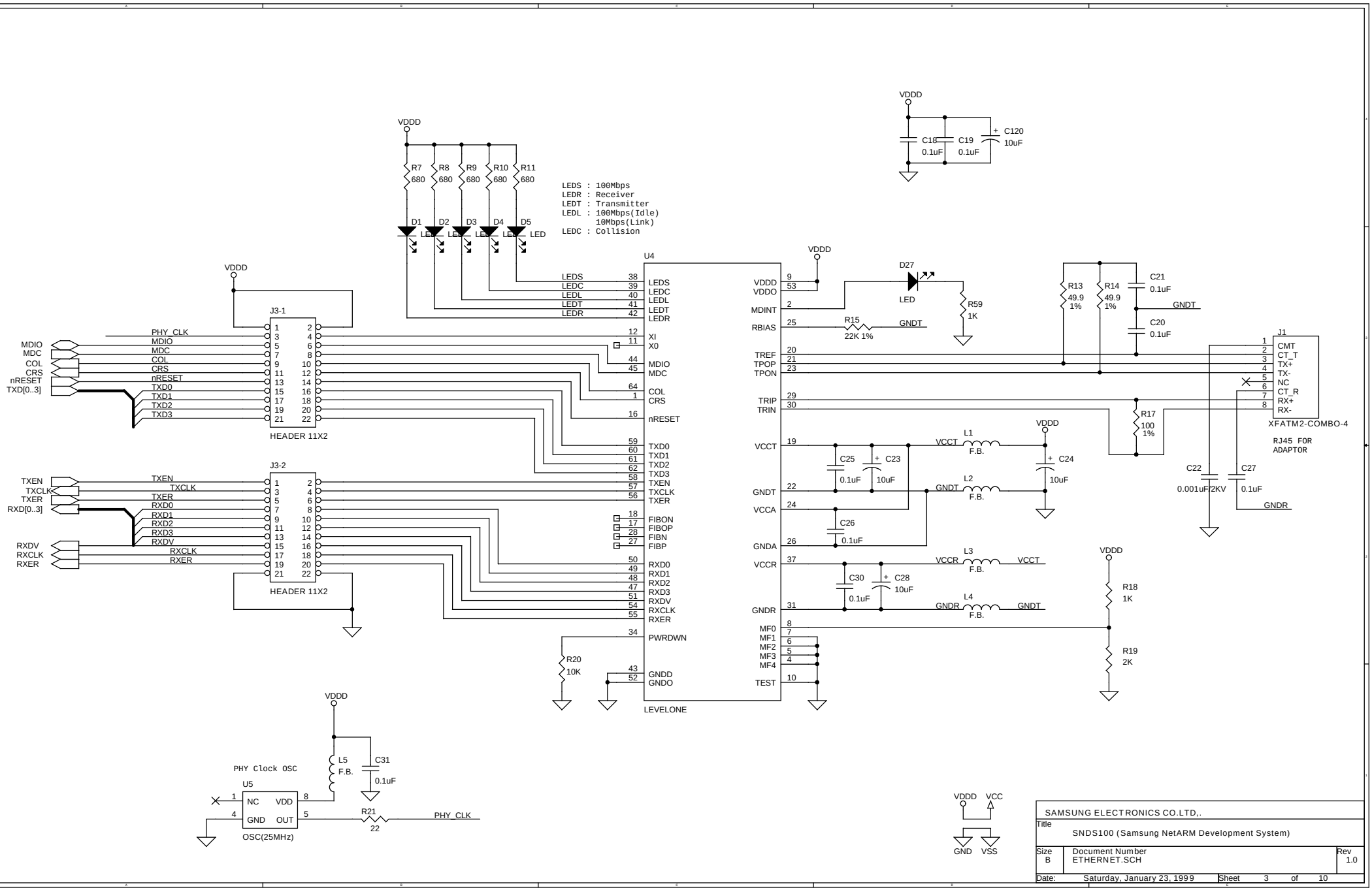

XDATA[0..31]
ADDR[0..13]
U1
U2
U3
VDD33
VDDD
KM416S4020B
DRAM_SIMM
nDWE
SDCLK(MCLKO)
nWBE[0..3]
R51 22
R61 22
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17
0.1uF
nRAS[0..3]
nCAS[0..3]
JP1
JP2
HEADER 4X2
R1 22 nSDCS
R4 22 nRAS
R2 22 nSDRAS(nCAS0)
R3 22 nSDCAS(nCAS1)
R5 22 CKE(nCAS2)
R6 22 T(nCAS3)
VDDD VCC
GND VSS
SAMSUNG ELECTRONICS CO.LTD,.
SNDS100 (Samsung NetARM Development System)
Size B
Document Number DRAM.SCH
Rev 1.0
Date: Thursday, January 21, 1999
Sheet 2 of 10


VDDD
R7 680
R8 680
R9 680
R10 680
R11 680
D1 LED
D2 LED
D3 LED
D4 LED
D5 LED
LEDS : 100Mbps
LEDR : Receiver
LEDT : Transmitter
LEDL : 100Mbps(Idle)
10Mbps(Link)
LEDC : Collision
C18 0.1uF
C19 0.1uF
C120 10uF
U4
LEDS 38
LEDC 39
LEDL 40
LEDT 41
LEDR 42
XI 12
X0 11
MDIO 44
MDC 45
COL 64
CRS 1
nRESET 16
TXD0 59
TXD1 60
TXD2 61
TXD3 62
TXEN 58
TXCLK 57
TXER 56
FIBON 18
FIBOP 17
FIBN 28
FIBP 27
RXD0 50
RXD1 49
RXD2 48
RXD3 47
RXDV 51
RXCLK 54
RXER 55
PWRDWN 34
GNDD 43
GNDO 52
LEVELONE
VDDD 9
VDDO 53
MDINT 2
RBIAS 25
TREF 20
TPOP 21
TPON 23
TRIP 29
TRIN 30
VCCT 19
GNDT 22
VCCA 24
GNDA 26
VCCR 37
GNDR 31
MF0 8
MF1 7
MF2 6
MF3 5
MF4 4
TEST 10
D27 LED
R59 1K
R15 22K 1%
GNDT
R13 49.9 1%
R14 49.9 1%
C21 0.1uF
C20 0.1uF
J1
CMT 1
CT_T 2
TX+ 3
TX- 4
NC 5
CT_R 6
RX+ 7
RX- 8
XFATM2-COMBO-4
RJ45 FOR ADAPTOR
R17 100 1%
C22 0.001uF/2KV
C27 0.1uF
GNDR
L1 F.B.
L2 F.B.
L3 F.B.
L4 F.B.
C25 0.1uF
C23 10uF
C24 10uF
C26 0.1uF
C30 0.1uF
C28 10uF
R18 1K
R19 2K
R20 10K
J3-1
PHY_CLK
MDIO
MDC
COL
CRS
nRESET
TXD0
TXD1
TXD2
TXD3
HEADER 11X2
J3-2
TXEN
TXCLK
TXER
RXD0
RXD1
RXD2
RXD3
RXDV
RXCLK
RXER
HEADER 11X2
PHY Clock OSC
U5
NC
VDD
GND
OUT
OSC(25MHz)
L5 F.B.
C31 0.1uF
R21 22
PHY_CLK
VDDD VCC
GND VSS
SAMSUNG ELECTRONICS CO.LTD,.
Title
SNDS100 (Samsung NetARM Development System)
Size B
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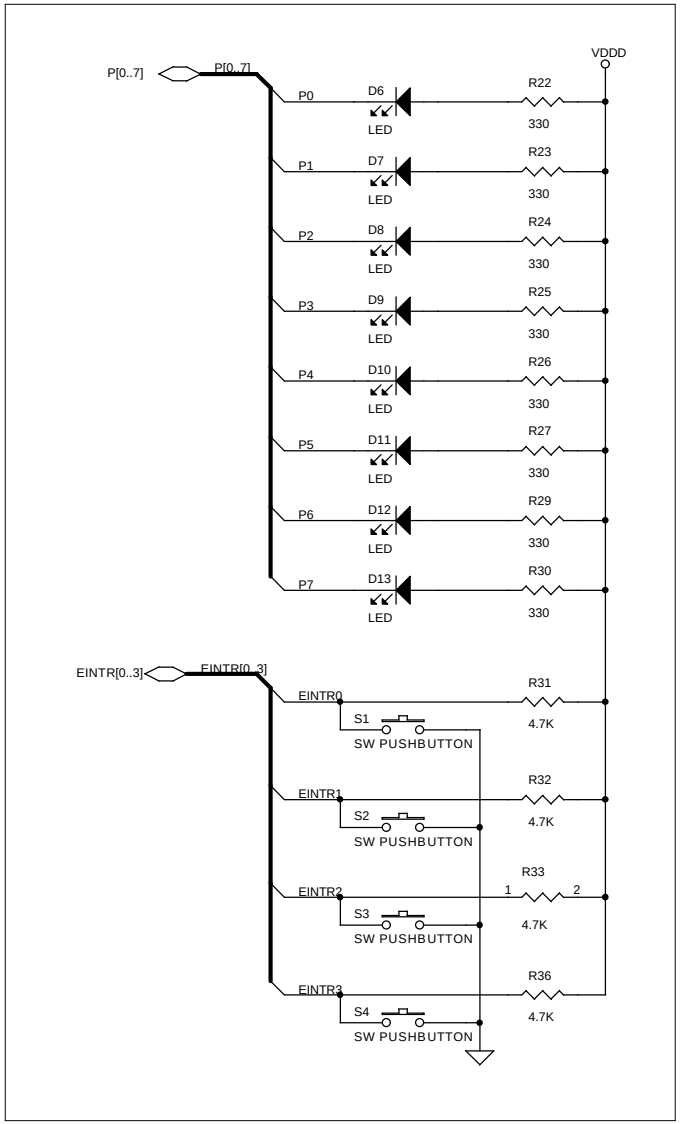

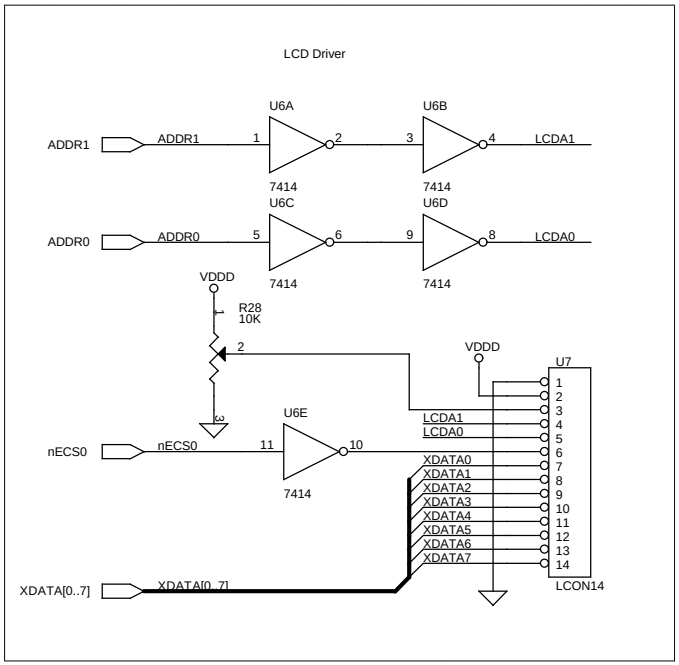

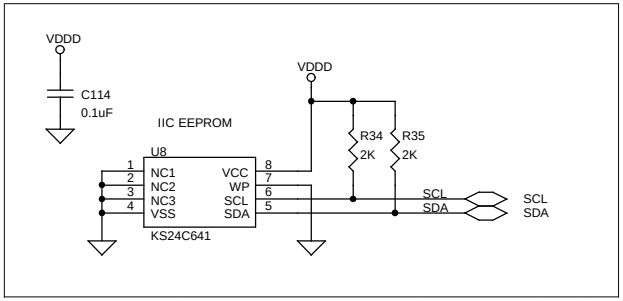

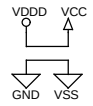

SAMSUNG ELECTRONICS CO.LTD,.		
Title: SNDS100 (Samsung NetARM Development System)		
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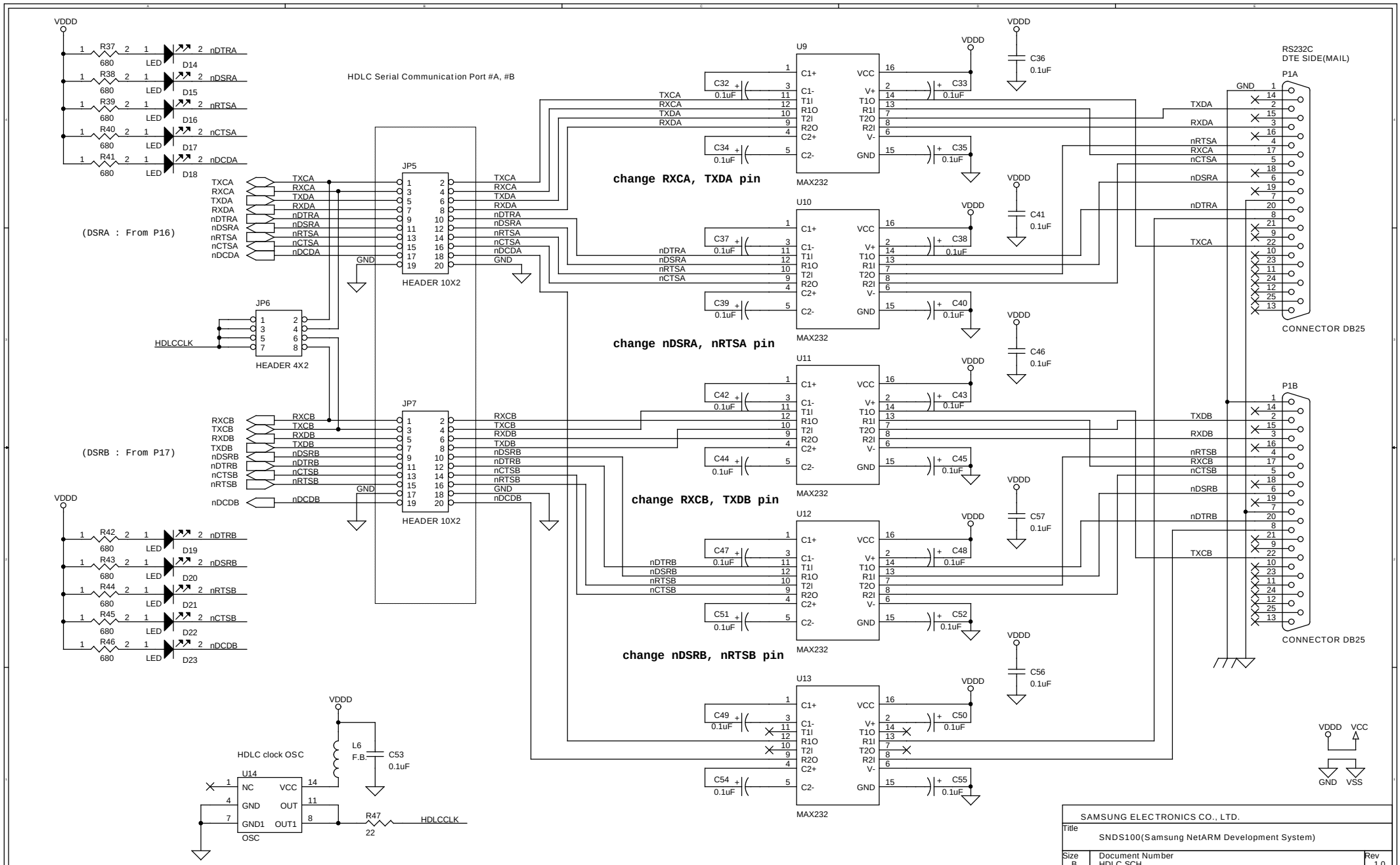
HDLC Serial Communication Port #A, #B
VDDD
R37 680
R38 680
R39 680
R40 680
R41 680
LED
D14
D15
D16
D17
D18
nDTRA
nDSRA
nRTSA
nCTSA
nDCDA
(DSRA : From P16)
JP5
HEADER 10X2
JP6
HEADER 4X2
HDLCCLK
JP7
(DSRB : From P17)
R42 680
R43 680
R44 680
R45 680
R46 680
D19
D20
D21
D22
D23
nDTRB
nDSRB
nRTSB
nCTSB
nDCDB
HDLC clock OSC
U14
NC
GND
GND1
VCC
OUT
OUT1
OSC
L6
F.B.
C53
0.1uF
R47
22
HDLCCLK
U9
U10
U11
U12
U13
MAX232
C1+
C1-
T1I
R1O
T2I
R2O
C2+
C2-
VCC
V+
T1O
R1I
T2O
R2I
V-
GND
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C54
C55
C56
C57
change RXCA, TXDA pin
change nDSRA, nRTSA pin
change RXCB, TXDB pin
change nDSRB, nRTSB pin
RS232C
DTE SIDE(MAIL)
P1A
P1B
CONNECTOR DB25
SAMSUNG ELECTRONICS CO., LTD.
SNDS100(Samsung NetARM Development System)
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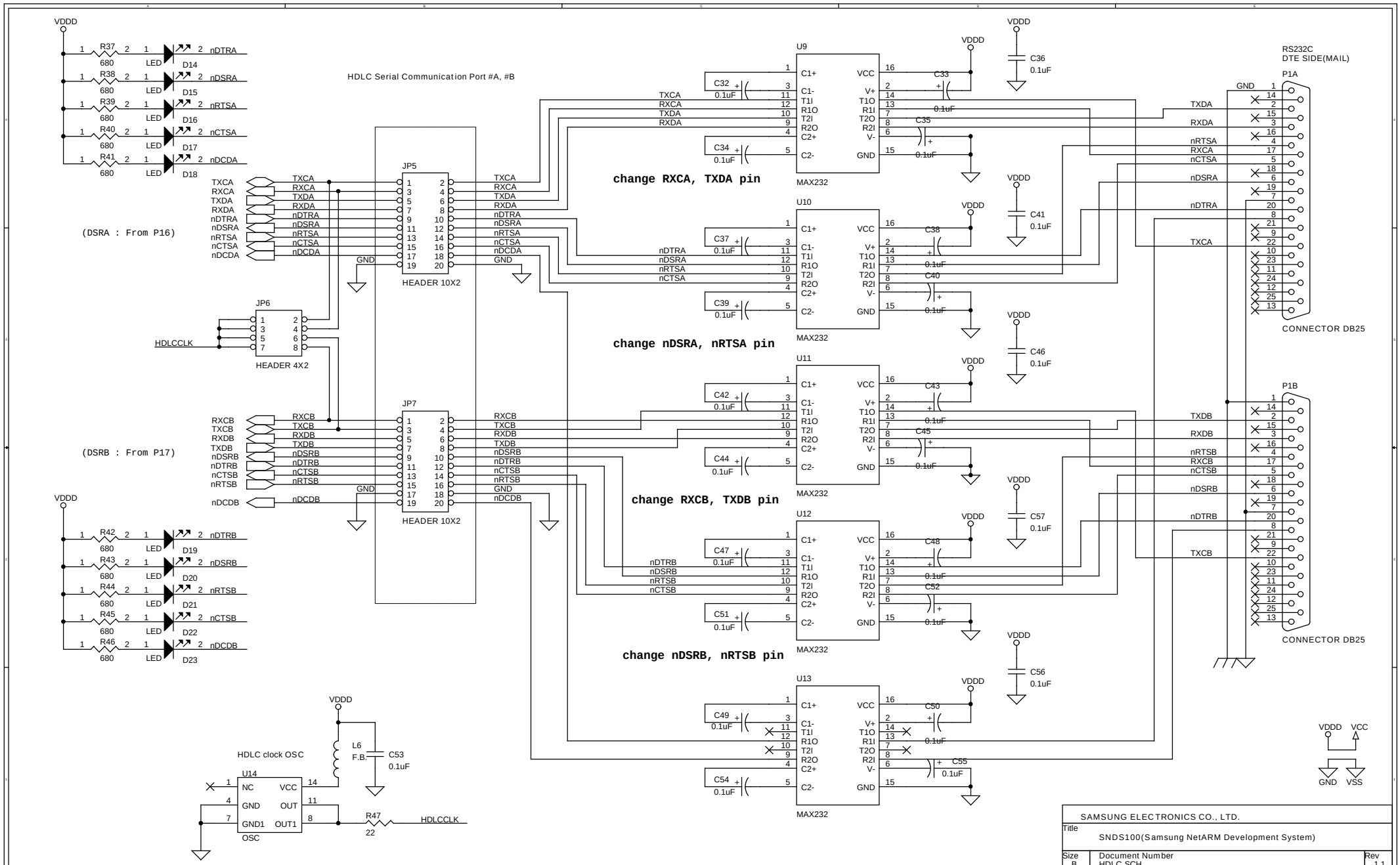
HDLC Serial Communication Port #A, #B
VDDD
R37 680 LED D14 nDTRA
R38 680 LED D15 nDSRA
R39 680 LED D16 nRTSA
R40 680 LED D17 nCTSA
R41 680 LED D18 nDCDA
(DSRA : From P16)
TXCA RXCA TXDA RXDA nDTRA nDSRA nRTSA nCTSA nDCDA
JP5
HEADER 10X2
GND
JP6
HDLCCLK
HEADER 4X2
(DSRB : From P17)
RXCB TXCB RXDB TXDB nDSRB nDTRB nCTSB nRTSB nDCDB
JP7
HEADER 10X2
R42 680 LED D19 nDTRB
R43 680 LED D20 nDSRB
R44 680 LED D21 nRTSB
R45 680 LED D22 nCTSB
R46 680 LED D23 nDCDB
HDLC clock OSC
U14
NC VCC GND OUT GND1 OUT1
OSC
L6 F.B.
C53 0.1uF
R47 22 HDLCCLK
U9
U10
U11
U12
U13
C1+ C1- T1I R1O T2I R2O C2+ C2- VCC V+ T1O R1I T2O R2I V- GND
C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C54 C55 C56 C57 0.1uF
MAX232
change RXCA, TXDA pin
change nDSRA, nRTSA pin
change RXCB, TXDB pin
change nDSRB, nRTSB pin
RS232C
DTE SIDE(MAIL)
P1A
P1B
CONNECTOR DB25
TXDA RXDA nRTSA RXCA nCTSA nDSRA nDTRA TXCA
TXDB RXDB nRTSB RXCB nCTSB nDSRB nDTRB TXCB
VDDD VCC
GND VSS
SAMSUNG ELECTRONICS CO., LTD.
Title
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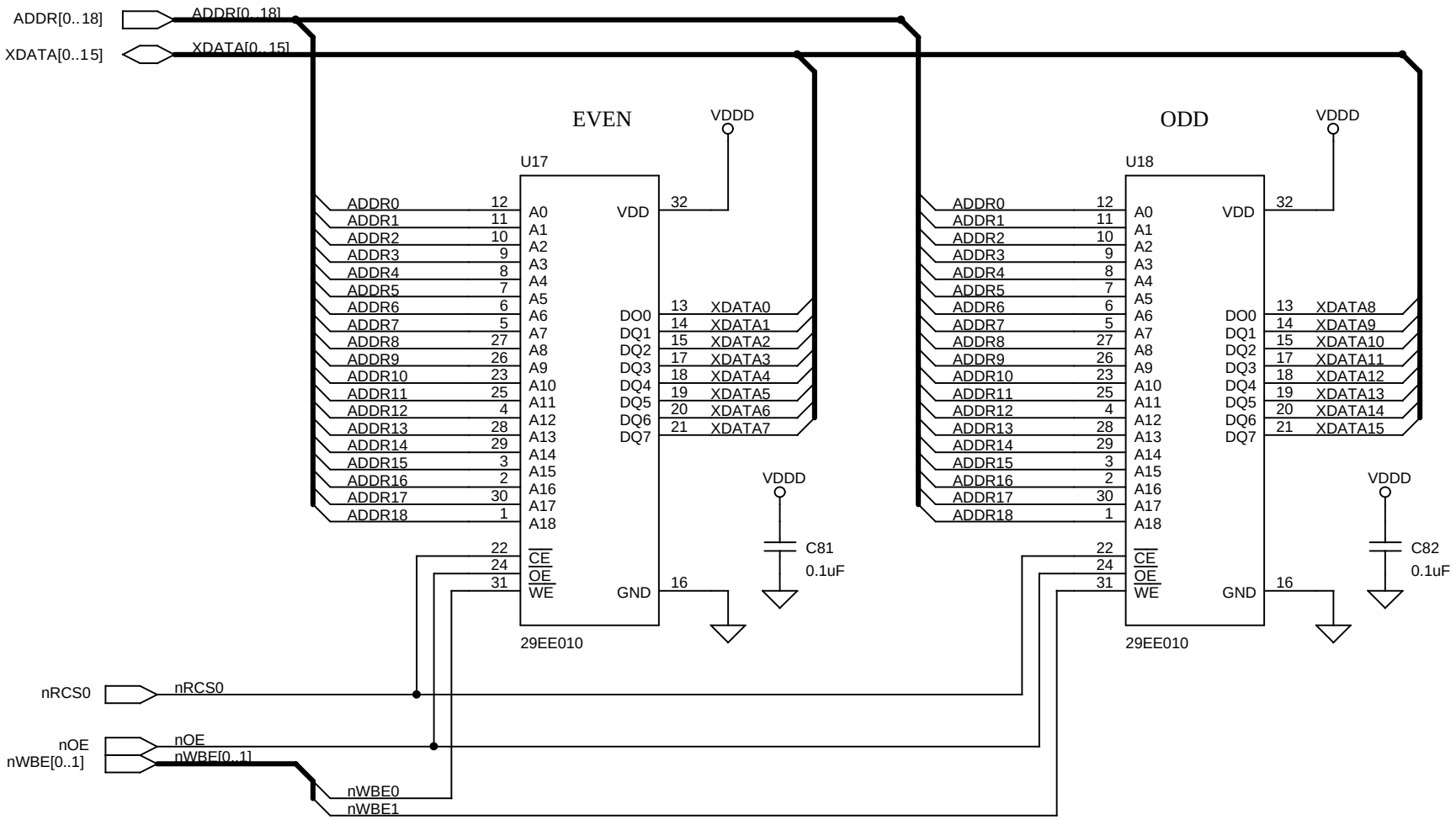
Boot Flash ROM : 8/16 Bit Bus Width is Selectable



SAMSUNG ELECTRONICS CO .LTD,.		
Title: SNDS100 (Samsung NetARM Development System)		
Size: A	Document Number: ROM.SCH	Rev: 1.0
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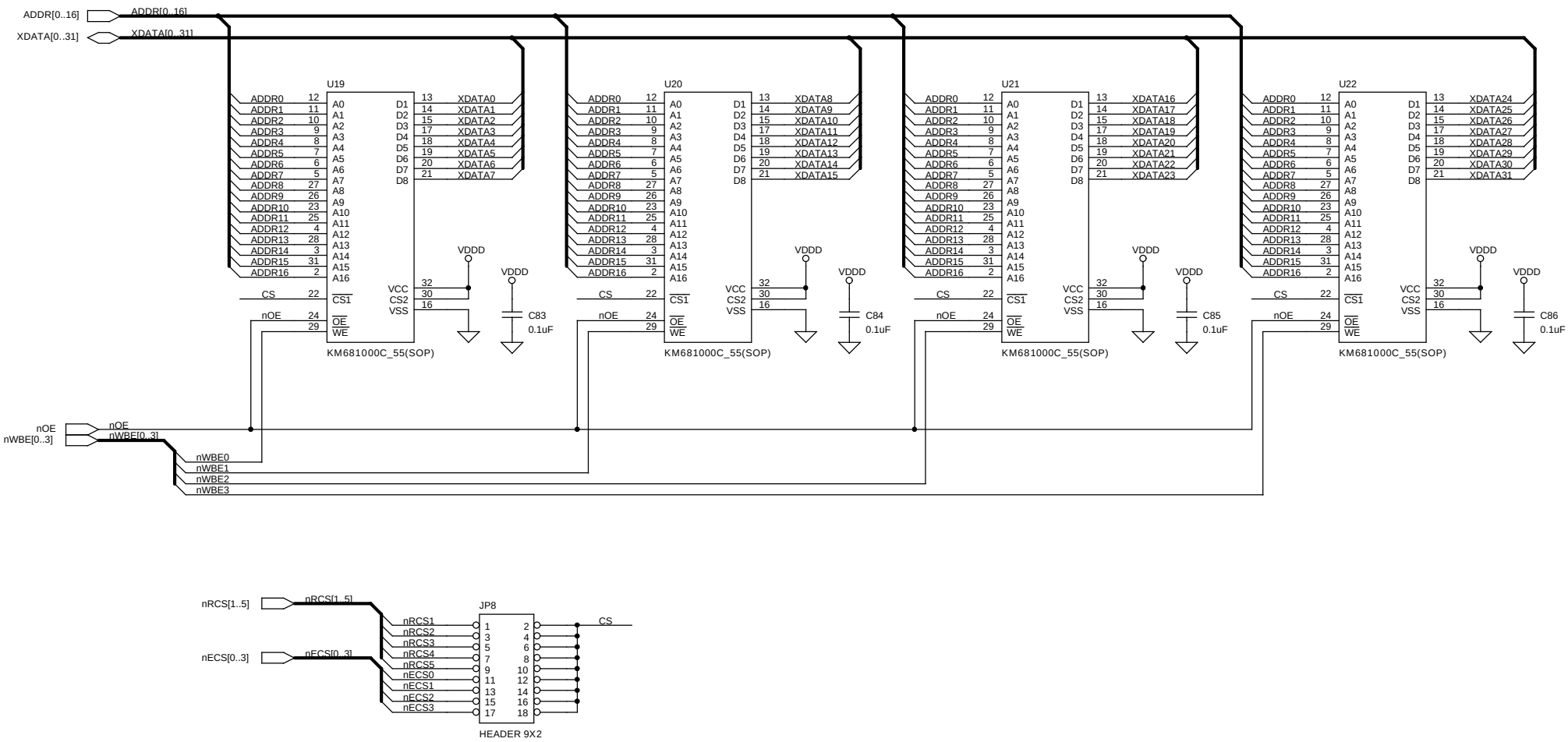

SAMSUNG ELECTRONICS CO.LTD,.

Title: SNDS100 (Samsung NetARM Development System)

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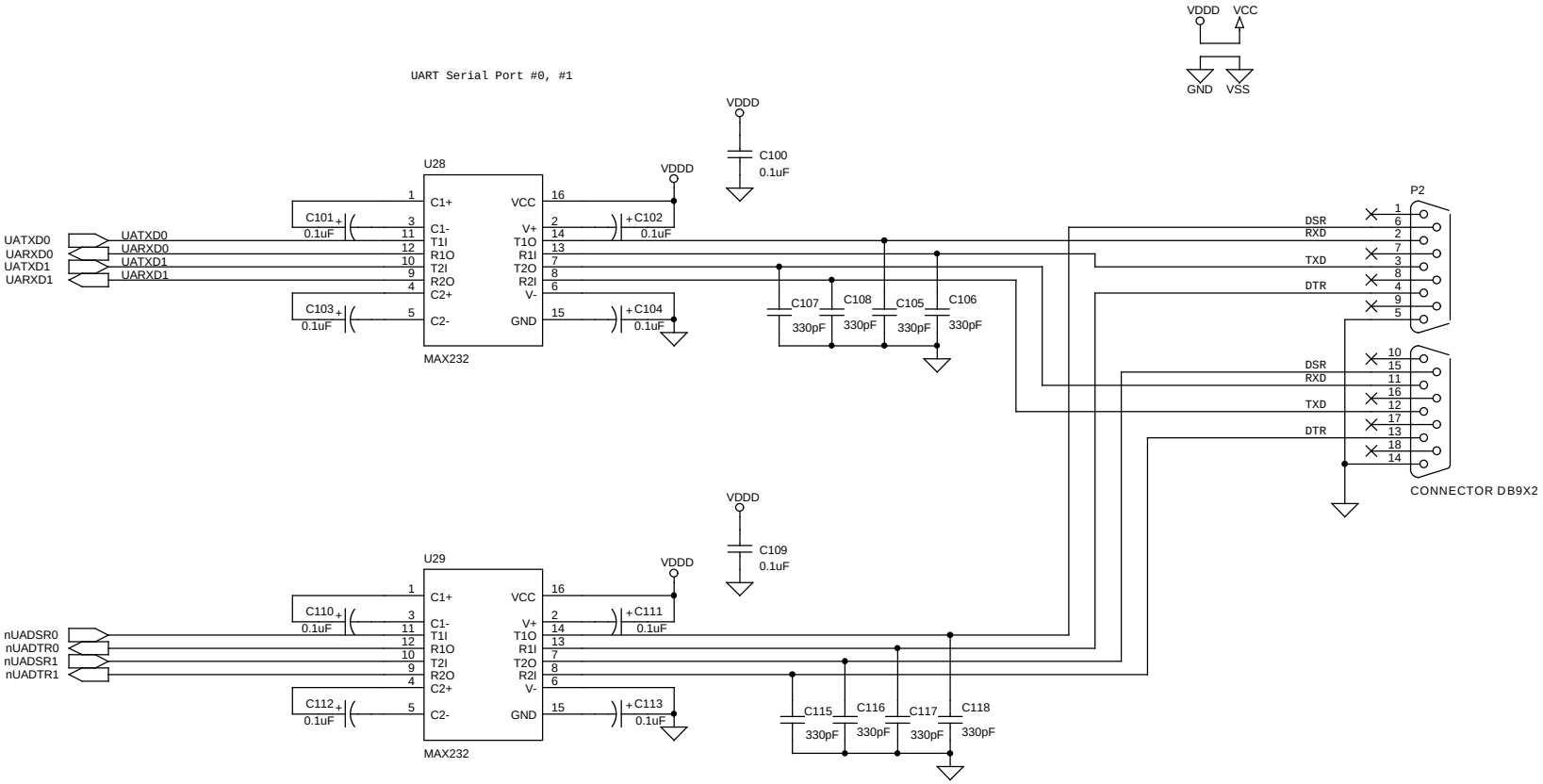

SAMSUNG ELECTRONICS CO.LTD,.		
Title: SNDS100 (Samsung NetARM Development System)		
Size: B	Document Number: UART.SCH	Rev: 1.0
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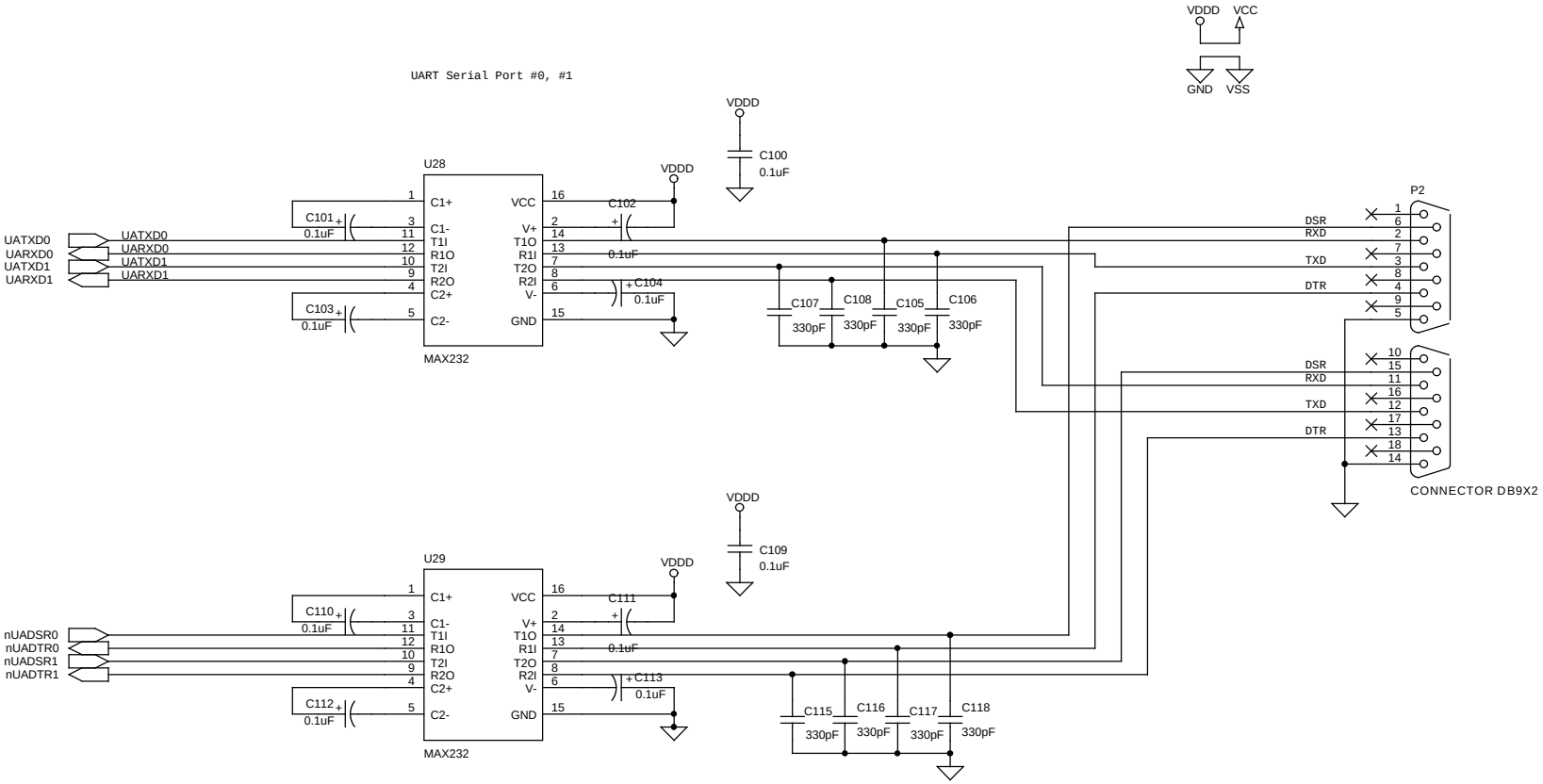

SAMSUNG ELECTRONICS CO.LTD,.		
Title: SNDS100 (Samsung NetARM Development System)		
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